

**WHAT IS CLAIMED IS:**

1. A process for using a photo-definable layer in a negative mask scheme to manufacture a semiconductor device, comprising:

5 forming over a substrate a photo-definable layer that is convertible to an insulative material;

exposing selected portions of said photo-definable layer to electro-magnetic radiation in a negative pattern scheme to convert said selected portions to an insulative material;

removing exposed portions of said photo-definable layer with an etch process that is

10 selective to non-exposed portions of said photo-definable layer; and

using said non-exposed portions of said photo-definable layer as a patterned mask for further processing steps.

2. The process of claim 1, wherein said photo-definable layer comprises an organosilicon  
15 resist.

3. The process of claim 2, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS) and said insulative material comprises photo-oxidized siloxane (PPMSO).

20 4. The process of claim 3, wherein said substrate comprises an oxide layer underlying said photo-definable layer.

5. The process of claim 4, wherein said removing step removes said exposed portions and portions of said oxide layer underlying said exposed portions in a single etch step.

6. A semiconductor device formed using a photo-definable layer in a negative mask scheme,

5 comprising:

a substrate; and

at least one feature formed on said substrate by converting selected portions of a photo-definable layer to an insulative material through exposure to electro-magnetic radiation in a negative mask scheme and by using non-exposed portions of said photo-definable layer as a mask to form said at least one feature.

7. The semiconductor device of claim 6, further comprising an insulative layer formed on said substrate from said non-exposed portions of said photo-definable layer that were subsequently converted to an insulative layer through exposure to electro-magnetic radiation.

8. The semiconductor device of claim 7, wherein said photo-definable layer comprises an organosilicon resist.

9. The semiconductor device of claim 8, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS).

10. The semiconductor device of claim 9, wherein said feature is part of a memory cell array.

11. A process for etching an insulative layer using a photo-definable layer in a negative mask scheme, comprising:

forming over an insulative layer a photo-definable layer that is convertible to an insulative material;

5 exposing selected portions of said photo-definable layer to electro-magnetic radiation in a negative pattern scheme to convert said selected portions to an insulative material; and

removing exposed portions of said photo-definable layer and underlying portions of said insulative layer with a single-step etch process that is selective to non-exposed portions of said photo-definable layer such that said non-exposed portions of said photo-definable layer act as a patterned mask in a negative pattern scheme.

12. The process of claim 11, wherein said photo-definable layer comprises an organosilicon resist.

13. The process of claim 12, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS) and said insulative material comprises photo-oxidized siloxane (PPMSO).

14. The process of claim 13, further comprising, after said removing step, converting said non-exposed PPMS portions to a PPMSO layer through exposure to ultra-violet radiation in the presence oxygen, converting said PPMSO layer to oxide through exposure to an oxygen plasma, and leaving said oxide as a feature on said substrate.

15. The process of claim 13, wherein said insulative layer comprises an oxide layer.

16. The process of claim 15, wherein said exposed portions of said photo-definable layer are  
5 removed using an oxide etch.

17. The process of claim 11, wherein said removing step forms a plurality of trenches within  
said insulative layer.

18. The process of claim 17, wherein said plurality of trenches are within a memory cell  
10 array.

19. A patterned insulative structure within a semiconductor device formed using a photo-  
definable layer in a negative mask scheme, comprising:

15 a substrate; and

a patterned insulative layer formed on said substrate by converting selected portions of a  
photo-definable layer to an insulative material through exposure to electro-  
magnetic radiation in a negative mask scheme and by using non-exposed portions  
of said photo-definable layer as a mask to form said patterned insulative layer.

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20. The patterned insulative structure of claim 19, wherein said insulative layer comprises an  
oxide layer.

21. The patterned insulative structure of claim 20, wherein said photo-definable layer comprises an organosilicon resist.

22. The patterned insulative structure of claim 21, wherein said photo-definable layer  
5 comprises plasma polymerized methylsilane (PPMS).

23. The patterned insulative structure of claim 22, wherein said insulative layer comprises a plurality of trench structures within a memory cell array.

24. The patterned insulative structure of claim 23, wherein said patterned insulative layer  
10 comprises non-exposed portions of said photo-definable layer that were converted into additional insulative material after formation of said patterned insulative layer.

25. A process for etching an insulative layer followed by a conductive layer in the  
15 manufacture of a semiconductor device, comprising:

forming an insulative layer over a conductive layer on a substrate;

forming over said insulative layer a photo-definable layer that is convertible to an  
insulative material;

exposing selected portions of said photo-definable layer to electro-magnetic radiation to

20 convert said selected portions to an insulative material;

removing exposed portions of said photo-definable layer and underlying portions of said

insulative layer with a single-step etch process that is selective to non-exposed

portions of said photo-definable layer to form a void within said insulative layer;

and

removing a portion of said conductive layer within said void.

5 26. The process of claim 25, wherein said removing steps are performed without removing said substrate from a processing chamber.

27. The process of claim 25, wherein remaining portions of said photo-definable layer are also removed as a sacrificial layer during said second removing step.

28. The process of claim 26, wherein said photo-definable layer comprises an organosilicon resist.

29. The process of claim 28, wherein said photo-definable layer comprises plasma  
15 polymerized methylsilane (PPMS) and said insulative material comprises photo-oxidized siloxane (PPMSO).

30. The process of claim 29 wherein said exposing step is performed by irradiating said selected portions of said photo-definable layer with ultraviolet light in the presence oxygen.

20 31. The process of claim 29, wherein said insulative layer comprises an oxide layer.

32. The process of claim 31, wherein said exposed portions of said photo-definable layer and said underlying portion of said oxide layer are removed using a single-step oxide etch.

33. The process of claim 25, further comprising depositing a conductive material within said  
5 void to form an interconnect structure.

34. A conductive interconnect structure within a semiconductor device formed using a photo-definable layer, comprising:

a substrate;

10 a first conductive layer over said substrate;

an insulative layer over said conductive layer; and

a second conductive layer formed within a desired portion of said insulative layer to

create a conductive interconnect structure connected to said first conductive layer,

said second conductive layer being formed by converting selected portions of a

15 photo-definable layer to an insulative material through exposure to electro-

magnetic radiation in a negative mask scheme, by using non-exposed portions of

said photo-definable layer as a mask to form a pattern within said insulative layer,

and by using non-exposed portions of said photo-definable layer as a sacrificial

mask in etching said second conductive layer.

20 35. The conductive interconnect structure of claim 34, wherein said photo-definable layer comprises an organosilicon resist.

36. The conductive interconnect structure of claim 35, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS).

37. The conductive interconnect structure of claim 34, wherein said substrate includes a plurality of transistor gate structures for a memory cell array.

38. A process of using a photo-definable layer to underlie an organic photoresist layer during the manufacture of an integrated circuit structure, comprising

forming over an insulative layer a photo-definable layer that is convertible to an

insulative material;

creating a patterned organic photoresist layer over said photo-definable layer to leave

unmasked portions of said photo-definable layer;

exposing selected portions of said photo-definable layer to electro-magnetic radiation to

convert said selected portions to an insulative material;

removing exposed portions of said photo-definable layer and underlying portions of said

insulative layer with an etch process that is selective to non-exposed portions of

said photo-definable layer to form a void within said insulative layer.

39. The process of claim 38, further comprising stripping said organic photoresist prior to said removing step.

40. The process of claim 38, further comprising stripping said organic photoresist after said removing step.

41. The process of claim 38, further comprising exposing remaining portions of said photo-definable layer to serve as an additional insulative material for said insulative layer.

5 42. The process of claim 41, wherein said photo-definable layer comprises an organosilicon resist.

43. The process of claim 42, wherein said photo-definable layer comprises plasma  
polymerized methylsilane (PPMS) and said insulative material comprises photo-oxidized  
10 siloxane (PPMSO).

44. The process of claim 43, further comprising converting said non-exposed PPMS portions  
to a PPMSO layer through exposure to ultraviolet light and converting said PPMSO layer to  
oxide through exposure to an oxygen plasma.

15 45. The process of claim 38, wherein said exposing step is performed by irradiating said  
selected portions of said photo-definable layer with ultraviolet light in the presence oxygen.

46. The process of claim 45, wherein said insulative layer comprises an oxide layer.

20 47. The process of claim 46, wherein said exposed portions of said photo-definable layer are  
removed using an oxide etch.

48. The process of claim 47, wherein said removing step forms a plurality of trench structures within said oxide layer, said plurality of trench structures being within a memory cell array.

49. A patterned insulative structure within a semiconductor device using a photo-definable

5 layer as a mask layer, comprising:

a substrate; and

an insulative layer on said substrate formed by covering a photo-definable layer with a

patterned organic photoresist, by converting unmasked portions of a photo-

definable layer to an insulative material through exposure to electro-magnetic

10 radiation in a negative mask scheme, and by using non-exposed portions of said

photo-definable layer and said organic photoresist as a mask to form a pattern

within said insulative layer.

50. The patterned insulative structure of claim 49, wherein said photo-definable layer

15 comprises an organosilicon resist.

51. The patterned oxide structure of claim 50, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS).

20 52. The patterned insulative structure of claim 51, wherein said insulative layer comprises an oxide layer.

53. The patterned insulative structure of claim 52, wherein said insulative layer comprises a plurality of trench structures within a memory cell array.

54. The patterned insulative structure of claim 49, wherein said insulative layer comprises non-exposed portions of said photo-definable layer subsequently converted into additional insulative material.

55. A process for using a photo-definable layer in a positive mask scheme to manufacture a semiconductor device, comprising:

forming over a substrate a photo-definable layer that is convertible to an insulative material;

exposing selected portions of said photo-definable layer to electro-magnetic radiation in a positive pattern scheme to convert said selected portions to an insulative material;

removing non-exposed portions of said photo-definable layer with an etch process that is selective to exposed portions of said photo-definable layer;

using said non-exposed portions of said photo-definable layer as a patterned mask for further processing steps, and

leaving said exposed portions of said photo-definable layer as an insulative layer within said semiconductor device.

56. The process of claim 55, wherein said photo-definable layer comprises an organosilicon resist.

57. The process of claim 56, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS) and said insulative material comprises photo-oxidized siloxane (PPMSO).

5 58. The process of claim 57, further comprising converting said PPMSO layer to oxide through exposure to an oxygen plasma.

59. A semiconductor device formed using a photo-definable layer in a positive mask scheme, comprising:

10 a substrate;

at least one feature formed on said substrate by converting selected portions of a photo-definable layer to an insulative material through exposure to electro-magnetic radiation in a negative mask scheme, by using exposed portions of said photo-definable layer as a mask to form said at least one feature, and by leaving said exposed portions of said photo-definable layer on said substrate as an insulative layer.

60. The semiconductor memory device of claim 59, wherein said photo-definable layer comprises an organosilicon resist.

20 61. The semiconductor memory device of claim 60, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS).

62. A process for forming a self-aligned contact during the manufacture of a semiconductor device using a photo-definable layer in a positive mask scheme, comprising:

forming an insulative layer over a substrate having at least two spaced structures;

forming over said insulative layer a photo-definable layer that is convertible to an

5 insulative material;

exposing selected portions of said photo-definable layer to electro-magnetic radiation in a

positive pattern scheme to convert said selected portions to an insulative material;

removing non-exposed portions of said photo-definable layer with an etch process that is

selective to exposed portions of said photo-definable layer to expose selected

10 portions of said insulative layer between said spaced structures;

removing said selected portions of said insulative layer to expose underlying portions of

said substrate; and

depositing conductive material to form a self-aligned contact between said spaced

structures.

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63. The process of claim 62, wherein said photo-definable layer comprises an organosilicon resist.

64. The process of claim 63, wherein said photo-definable layer comprises plasma

20 polymerized methylsilane (PPMS) and said insulative material comprises photo-oxidized siloxane (PPMSO).

65. The process of claim 64, further comprising converting said PPMSO to an oxide layer by exposure to oxygen plasma and consolidating said oxide layer with an anneal.

66. The process of claim 62, wherein said exposing step is performed by irradiating said  
5 selected portions of said photo-definable layer with ultraviolet light in the presence oxygen.

67. The process of claim 66, wherein said non-exposed portions of said photo-definable layer are removed using a chlorine-based or a bromine-based plasma etch.

68. The process of claim 66, wherein said insulative layer comprises an oxide layer and said  
10 insulative layer is removed using a short punch-through oxide etch.

69. The process of claim 62, wherein said spaced structures comprise transistor gate  
structures that are part of a memory cell array.

70. The process of claim 69, wherein said gate structure comprise a polysilicon layer and said  
15 insulative layer comprises an oxide layer.

71. A self-aligned contact structure within a semiconductor device formed using a photo-  
20 definable layer in a positive mask scheme, comprising:

a substrate; and

at least one self-aligned contact formed on said substrate by converting selected portions  
of a photo-definable layer to an insulative material through exposure to electro-

magnetic radiation in a positive mask scheme and by using exposed portions of  
said photo-definable layer as a mask to form said at least one self-aligned contact.

72. The self-aligned contact structure of claim 71, further comprising an insulative layer  
5 formed by leaving said exposed portions of said photo-definable layer on said substrate.

73. The self-aligned contact structure of claim 72, wherein said photo-definable layer  
comprises an organosilicon resist.

74. The self-aligned contact structure of claim 73, wherein said photo-definable layer  
10 comprises plasma polymerized methylsilane (PPMS).

75. The self-aligned contact structure of claim 71, where said at least one self-aligned contact  
lies between two transistor gate structures within a memory cell array.

76. A process of using a photo-definable layer in a Damascene process to create a patterned  
structure, comprising:

forming on a substrate a photo-definable layer that is convertible to an insulative  
material;

20 exposing selected portions of said photo-definable layer to electro-magnetic radiation to  
convert said selected portions to an insulative material;

removing non-exposed portions of said photo-definable layer with an etch process that is selective to exposed portions of said photo-definable layer to form a desired pattern within said exposed portions of said photo-definable layer; and leaving said exposed portions of said photo-definable layer on said substrate as an insulative layer.

77. The process of claim 76, wherein said photo-definable layer comprises an organosilicon resist.

78. The process of claim 77, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS) and said insulative material comprises photo-oxidized siloxane (PPMSO).

79. The process of claim 78, further comprising converting said PPMSO to an oxide layer by exposure to oxygen plasma and consolidating said oxide layer with an anneal.

80. The process of claim 79, further comprising depositing a conductive material within said pattern.

81. The process of claim 80, wherein said conductive material forms an interconnect structure within a semiconductor memory device.

82. The process of claim 76, wherein said exposing step is performed by irradiating said selected portions of said photo-definable layer with ultraviolet light in the presence oxygen.

83. The process of claim 82, wherein said non-exposed portions of said photo-definable layer are removed using a chlorine-based or a bromine-based plasma etch.

84. A conductive interconnect structure within a semiconductor device formed using a photo-definable layer, comprising:

a substrate;

a patterned insulative layer on said substrate formed by converting selected portions of a photo-definable layer to an insulative material through exposure to electromagnetic radiation in a positive mask scheme, by removing non-exposed portions of said photo-definable layer to form a pattern within said photo-definable layer, and by leaving said exposed portions of said photo-definable layer as said patterned insulative layer; and

a conductive layer inlaid within said patterned insulative layer.

85. The semiconductor structure of claim 84, wherein said photo-definable layer comprises an organosilicon resist.

86. The semiconductor structure of claim 85, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS).

87. The semiconductor structure of claim 83, wherein said conductive layer forms an interconnect structure within a semiconductor memory device.

88. A process of using a photo-definable layer in a dual Damascene process to create a patterned structure, comprising:

forming over a conductive layer a first photo-definable layer that is convertible to an insulative material;

exposing selected portions of said first photo-definable layer to electro-magnetic radiation to convert said selected portions to an insulative material to define desired contact areas;

forming over said first photo-definable layer a second photo-definable layer that is convertible to an insulative material;

exposing selected portions of said second photo-definable layer to electro-magnetic radiation to convert said selected portions to an insulative material to define a desired interconnect pattern; and

removing non-exposed portions of said first and second photo-definable layers to form voids exposing said desired contact areas and said desired interconnect pattern.

89. A process of claim 88, further comprising removing non-exposed portions of said first photo-definable layer to expose said desired contact areas before forming said second photo-definable layer.

90. The process of claim 88, wherein said photo-definable layer comprises an organosilicon resist.

91. The process of claim 90, wherein said photo-definable layer comprises plasma  
5 polymerized methylsilane (PPMS) and said insulative material comprises photo-oxidized siloxane (PPMSO).

92. The process of claim 91, further comprising converting said PPMSO to an oxide layer by exposure to oxygen plasma and consolidating said oxide layer with an anneal.

93. The process of claim 92, further comprising depositing a conductive material within said  
10 voids.

94. The process of claim 93, wherein said conductive material forms digit-line connections  
15 for dynamic random access memory cells.

95. The process of claim 89, wherein said exposing steps are performed by irradiating said selected portions of said photo-definable layer with ultraviolet light in the presence oxygen.

20 96. The process of claim 95, wherein said non-exposed portions of said photo-definable layer are removed using a chlorine-based or a bromine-based plasma etch.

97. A conductive interconnect structure within a semiconductor device, comprising:

a substrate;

a first conductive layer on said substrate;

a patterned insulative layer on said first conductive layer formed by converting selected

portions of a photo-definable layer to an insulative material through exposure to

electro-magnetic radiation in a positive mask scheme, by removing non-exposed

portions of said photo-definable layer to form a pattern within said photo-

definable layer, and by leaving said exposed portions of said photo-definable layer

as said patterned insulative layer; and

a second conductive layer inlaid within said insulative layer forming contacts with

selected portions of said first conductive layer.

98. The semiconductor structure of claim 97, wherein said photo-definable layer comprises an organosilicon resist.

99. The semiconductor structure of claim 98, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS).

100. The semiconductor structure of claim 99, wherein said conductive layer forms an interconnect structure within a semiconductor memory device.